

L3264D37-BU1HDC9B 32x64 256 Megabyte DDR400 DDR SDRAM

FEATURES

- 184-pin Un-buffered 8-Byte Dual-In-Line DDR SDRAM
- One bank 32M × 64
- JEDEC standard Double Data Rate Synchronous DRAMs (DDR SDRAM)
- Single + 2.5 V (±0.2 V) power supply
- Built with 256 Mbit DDR SDRAMs organized as 32Mb x 8 in 66-Lead TSOPII package
- Programmable CAS Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL_2 compatible
- Serial Presence Detect with E²PROM
- Jedec standard reference layout
- Gold plated contacts

GENERAL DESCRIPTION

The L3264D37-BU1HDC9B is an industry standard 184-pin 8-byte Dual in-line Memory Module (DIMM) organized as 32M × 64 for main memory applications. The memory array is designed with 256Mbit Double Data Rate Synchronous DRAMs. A variety of decoupling capacitors are mounted on the PC board.

SERIAL PRESENCE-DETECT OPERATION

The module incorporates serial presence-detect (SPD). The first 128 bytes is programmed by Legend to identify the module type and various SDRAM organizations and timing parameters.

ABSOLUTE MAXIMUM RATINGS*

Input / Output voltage relative to V_{SS}: 0.5-3.6 V
 Power supply voltage on V_{DD}/V_{DDQ} to V_{SS}: 0.5-3.6 V
 Storage temperature range: -55 +125 °C
 Power dissipation: 8 W
 Data out current (short circuit): 50 mA

* Permanent device damage may occur if “Absolute Maximum Ratings” are exceeded. Functional operation should be restricted to recommended operation conditions. Exposure to higher than recommended voltage for extended periods of time affect device reliability

SUPPLY VOLTAGE LEVELS and DC OPERATING CONDITIONS

Parameter	Symbol	Limit Values			Unit
		min.	nom.	max.	
Device Supply Voltage	V _{DD}	2.5	2.6	2.7	V
Output Supply Voltage	V _{DDQ}	2.5	2.6	2.7	V
Input Reference Voltage	V _{REF}	0.49 x V _{DDQ}	0.5 x V _{DDQ}	0.51 x V _{DDQ}	V
Termination Voltage	V _{TT}	V _{REF} - 0.04	V _{REF}	V _{REF} +0.04	V
EEPROM supply voltage	V _{DDSPD}	2.5	2.6	3.6	V
DC Input Logic High	V _{IH} (DC)	V +0.15		V +0.3	V
DC Input Logic Low	V _{IL} (DC)	- 0.30		V _{REF} - 0.15	V
Input Leakage Current	I _{IL}	- 16		16	µA
Output Leakage Current	I _{OL}	- 5		5	µA

LEGEND

Performance Technology

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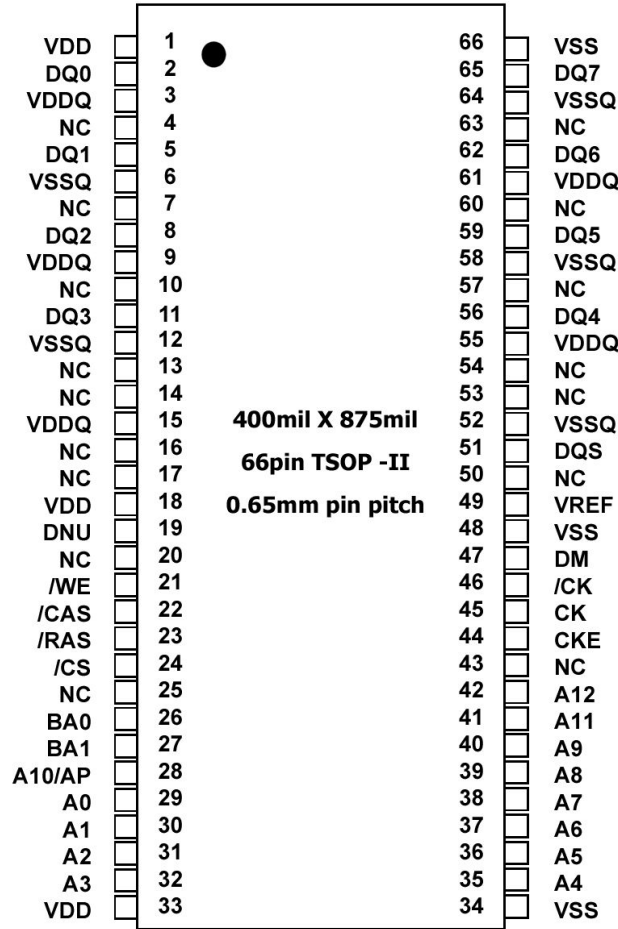
SPECIFICATIONS AND CONDITIONS

PARAMETER/CONDITION	SYMBOL		UNITS
Operating Current - One bank Active – Precharge	IDD0	720	mA
Operating Current - One bank Active / Read / Precharge	IDD1	960	
Precharge Power-Down Standby Current	IDD2P	160	
Precharge Floating Standby Current	IDD2F	320	
Active Power-Down Standby Current	IDD3P	200	
Active Standby Current	IDD3N	400	
Operating Current - Burst Read	IDD4R	1640	
Operating Current - Burst Write	IDD4W	1840	
Auto-Refresh Current	IDD5	1680	
Self-Refresh Current	IDD6	24	
Operating Current - Four bank operation	IDD7	2440	

SDRAM COMPONENT AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
t AC	DQ output access time from CK/CK	-0.7	0.7	ns
t DQSCK	DQS output access time from CK/CK	-0.55	0.55	ns
t CH	CK high-level width	0.45	0.55	t CK
t CL	CK low-level width	0.45	0.55	t CK
t HP	Clock Half Period	min (t CL, t CH)		ns
t CK	Clock cycle time	5	10	ns
t DH	DQ and DM input hold time	0.45		ns
t DS	DQ and DM input setup time	0.45		ns
t IPW	Control and Addr. input pulse width	2.2		ns
t HZ	Data-out high-impedence time from CK/CK	-0.7	0.7	ns
t LZ	Data-out low-impedence time from CK/CK	-0.7	0.7	ns
t DQSS	Write command to 1st DQS latching transition	0.75	1.25	t CK
t DQSQ	DQS-DQ skew (for DQS & associated DQ signals)		0.45	ns
t QHS	Data hold skew factor		0.55	ns
t QH	Data Output hold time from DQS	t HP - t QHS		ns
t DQSL,H	DQS input low (high) pulse width (write cycle)	0.35		t CK
t MRD	Mode register set command cycle time	2		t CK
t WPRES	Write preamble setup time	0		ns
t WPST	Write postamble	0.4	0.6	t CK
t WPRE	Write preamble	0.25		t CK
t IS	Address and control input setup time fast slew rate	fast slew rate	0.6	ns
		slow slew rate	0.7	ns
t IH	Address and control input hold time	fast slew rate	0.6	ns
		slow slew rate	0.7	ns
t RPRE	Read preamble	0.9	1.1	t CK
t RPST	Read postamble	0.4	0.6	t CK
t RAS	Active to Precharge command	40	70,000	ns
t RC	Active to Active/Auto-refresh command period	58		ns
t RFC	Auto-refresh to Active/Auto-refresh command period	70		ns
t RCD	Active to Read or Write delay	18		ns
t RP	Precharge command period	18		ns
t RRD	Active bank A to Active bank B command	10		ns
t WR	Write recovery time	15		ns
t DAL	Auto precharge write recovery + precharge time	(twr/tck) + (trp/tck)		t CK
t WTR	Internal write to read command delay	2		t CK
t REF1	Average Periodic Refresh Interval	7.8		μs
t XSC	Exit Self Refresh to Any Execute Command	200		t CK

DRAM PIN ASSIGNMENT



DRAM PIN Description

Pin	Description	Pin	Description
CK, /CK	Differential Clock Input	DM	Input Data Mask
CKE	Clock Enable Input	DQS	DATA Strobe I/O
/CS	Chip Select Input	DQ	DATA I/O
BA0, BA1	Bank Address Input	VDD, VSS, VDDQ, VSSQ	Power Supply
A0~A12	Address Input	VREF	Reference Voltage
/RAS, /CAS, /WE	Command Input	NS	No Connection

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MODULE PIN ASSIGNMENT

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREF	32	A5	62	VDDQ	93	VSS	124	VSS	154	/RAS
2	DQ0	33	DQ24	63	/WE	94	DQ4	125	A6	155	DQ45
3	VSS	34	VSS	64	DQ41	95	DQ5	126	DQ28	156	VDDQ
4	DQ1	35	DQ25	65	/CAS	96	VDDQ	127	DQ29	157	/CS0
5	DQS0	36	DQS3	66	VSS	97	DM0	128	VDDQ	158	/CS1
6	DQ2	37	A4	67	DQS5	98	DQ6	129	DM3	159	DM5
7	VDD	38	VDD	68	DQ42	99	DQ7	130	A3	160	VSS
8	DQ3	39	DDQ26	69	DQ43	100	VSS	131	DQ30	161	DQ46
9	NC	40	DDQ27	70	VDD	101	NC	132	VSS	162	DQ47
10	NC	41	A2	71	NC	102	NC	133	DQ31	163	NC
11	VSS	42	VSS	72	DQ48	103	A13*	134	CB4*	164	VDDQ
12	DQ8	43	A1	73	DQ49	104	VDDQ	135	CB5*	165	DQ52
13	DQ9	44	CB0*	74	VSS	105	DQ12	136	VDDQ	166	DQ53
14	DQS1	45	CB1*	75	/CK2	106	DQ13	137	CK0	167	NC
15	VDDQ	46	VDD	76	CK2	107	DM1	138	/CK0	168	VDD
16	CK1	47	DQS8*	77	VDDQ	108	VDD	139	VSS	169	DM6
17	/CK1	48	A0	78	DQS6	109	DQ14	140	DM8*	170	DQ54
18	VSS	49	CB2*	79	DQ50	110	DQ15	141	A10	171	DQ55
19	DQ10	50	VSS	80	DQ51	111	CKE1	142	CB6*	172	VDDQ
20	DQ11	51	CB3*	81	VSS	112	VDDQ	143	VDDQ	173	NC
21	CKE0	52	BA1	82	VDDID	113	BA2*	144	CB7*	174	DQ60
22	VDDQ	KEY		83	DQ56	114	DQ20	KEY		175	DQ61
23	DQ16	53	DQ32	84	DQ57	115	A12	145	VSS	176	VSS
24	DQ17	54	VDDQ	85	VDD	116	VSS	146	DQ36	177	DM7
25	DQS2	55	DQ33	86	DQS7	117	DQ21	147	DQ37	178	DQ62
26	VSS	56	DQS4	87	DQ58	118	A11	148	VDD	179	DQ63
27	A9	57	DQ34	88	DQ59	119	DM2	149	DM4	180	VDDQ
28	DQ18	58	VSS	89	VSS	120	VDD	150	DQ38	181	SA0
29	A7	59	BA0	90	WP	121	DQ22	151	DQ39	182	SA1
30	VDDQ	60	DQ35	91	SDA	122	A8	152	VSS	183	SA2
31	DQ19	61	DQ40	92	SCL	123	DQ23	153	DQ44	184	VDDSPD

MODULE PIN DESCRIPTION

Pin	Description	Pin	Description
CK0,/CK0,CK1,/CK1,CK2,/CK2	Differential Clock Inputs	VDDQ	DQs Power Supply
CS0	Chip Select Input	VSS	Ground
CKE0	Clock Enable Input	VREF	Reference Power Supply
/RAS, /CAS, /WE	Command Sets Inputs	VDDSPD	Power Supply for SPD
A0 ~ A12	Address	SA0~SA2	E 2 PROM Address Inputs
BA0, BA1	Bank Address	SCL	E 2 PROM Clock
DQ0~DQ63	Data Inputs/Outputs	SDA	E 2 PROM Data I/O
DQS0~DQS7	Data Strobe Inputs/Outputs	VDDID	VDD Identification Flag
DM0~DM7	Data-in Mask	DU	Do not Use
VDD	Power Supply	NC	No Connection

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MODULE METROLOGY

