

L6464S36-CA1HDK5A 64x64 512 Megabyte PC2700 DDR SDRAM SO-DIMM**FEATURES**

- 200-pin Un-buffered 8-Byte Dual-In-Line DDR SDRAM SO-DIMM
- Two bank 64M × 64
- JEDEC standard Double Data Rate Synchronous DRAMs (DDR SDRAM)
- Single + 2.5 V (±0.2 V) power supply
- Built with 512 Mbit DDR SDRAMs organized as 32Mb x 16 in 66-Lead TSOPII package
- Programmable CAS Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL_2 compatible
- Serial Presence Detect with E²PROM
- Jedec standard reference layout
- Gold plated contacts

GENERAL DESCRIPTION

The L6464S36-CA1HDK5A is an industry standard 200-pin 8-byte Dual in-line Memory Module (DIMM) organized as 64M × 64 for main memory applications. The memory array is designed with 512Mbit Double Data Rate Synchronous DRAMs. A variety of decoupling capacitors are mounted on the PC board.

SERIAL PRESENCE-DETECT OPERATION

The module incorporates serial presence-detect (SPD). The first 128 bytes is programmed by Legend to identify the module type and various SDRAM organizations and timing parameters.

ABSOLUTE MAXIMUM RATINGS*

Input / Output voltage relative to V_{SS}: 0.5-3.6 V
 Power supply voltage on V_{DD}/V_{DDQ} to V_{SS}: 0.5-3.6 V
 Storage temperature range: -55 +125 °C
 Power dissipation: 8 W
 Data out current (short circuit): 50 mA

* Permanent device damage may occur if "Absolute Maximum Ratings" are exceeded.
 Functional operation should be restricted to recommended operation conditions.
 Exposure to higher than recommended voltage for extended periods of time affect device reliability

SUPPLY VOLTAGE LEVELS and DC OPERATING CONDITIONS

Parameter	Symbol	Limit Values			Unit
		min.	nom.	max.	
Device Supply Voltage	V _{DD}	2.3	2.5	2.7	V
Output Supply Voltage	V _{DDQ}	2.3	2.5	2.7	V
Input Reference Voltage	V _{REF}	1.15	1.25	1.35	V
Termination Voltage	V _{TT}	V _{REF} - 0.04	V _{REF}	V _{REF} +0.04	V
EEPROM supply voltage	V _{DDSPD}	2.3	2.5	3.6	V
DC Input Logic High	V _{IH} (DC)	V +0.15		V +0.3	V
DC Input Logic Low	V _{IL} (DC)	- 0.30		V _{REF} - 0.15	V
Input Leakage Current	I _{IL}	- 32		32	µA
Output Leakage Current	I _{OL}	- 5		5	µA

LEGEND

Performance Technology

L6464S36-CA1HDK5A
256 Megabyte PC2700 DDR SDRAM

SPECIFICATIONS AND CONDITIONS

PARAMETER/CONDITION	SYMBOL	PC2700	UNITS
Operating Current - One bank Active – Precharge	IDD0	1040	mA
Operating Current - One bank Active / Read / Precharge	IDD1	1040	
Precharge Power-Down Standby Current	IDD2P	160	
Precharge Floating Standby Current	IDD2F	480	
Active Power-Down Standby Current	IDD3P	240	
Active Standby Current	IDD3N	560	
Operating Current - Burst Read	IDD4R	1440	
Operating Current - Burst Write	IDD4W	1520	
Auto-Refresh Current	IDD5	1520	
Self-Refresh Current	IDD6	48	
Operating Current - Four bank operation	IDD7	2240	

SDRAM COMPONENT AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
t AC	DQ output access time from CK/CK	-0.7	0.7	ns
t DQSCK	DQS output access time from CK/CK	-0.6	0.6	ns
t CH	CK high-level width	0.45	0.55	t CK
t CL	CK low-level width	0.45	0.55	t CK
t HP	Clock Half Period	min (t CL, t CH)		ns
t CK	Clock cycle time	6	12	ns
t IPW	Control and Addr. input pulse width	2.2		ns
t HZ	Data-out high-impedence time from CK/CK	-0.7	+0.7	ns
t LZ	Data-out low-impedence time from CK/CK	-0.7	+0.7	ns
t DQSQ	DQS-DQ skew (for DQS & associated DQ signals)		+0.45	ns
t QHS	Data hold skew factor		+0.55	ns
t QH	Data Output hold time from DQS	t HP - t QHS		ns
t IS	Address and control input setup time fast slew rate	fast slew rate	0.75	ns
		slow slew rate	0.8	ns
t IH	Address and control input hold time	fast slew rate	0.75	ns
		slow slew rate	0.8	ns
t RAS	Active to Precharge command	42	70,000	ns
t RC	Active to Active/Auto-refresh command period	60		ns
t RFC	Auto-refresh to Active/Auto-refresh command period	72		ns
t RCD	Active to Read or Write delay	18		ns
t RP	Precharge command period	18		ns
t RRD	Active bank A to Active bank B command	12		ns
t WR	Write recovery time	15		ns
t DAL	Auto precharge write recovery + precharge time	(twr/tck) + (trp/tck)		t CK
t WTR	Internal write to read command delay	1		t CK

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MODULE PIN ASSIGNMENT

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VREF	2	VREF	67	DQ27	68	DQ31	135	DQ34	136	DQ38
3	VSS	4	VSS	69	VDD	70	VDD	137	VSS	138	VSS
5	DQ0	6	DQ4	71	CB0*	72	CB4*	139	DQ35	140	DQ39
7	DQ1	8	DQ5	73	CB1*	74	CB5*	141	DQ40	142	DQ44
9	VDD	10	VDD	75	VSS	76	VSS	143	VDD	144	VDD
11	DQS0	12	DM0	77	DQS8*	78	DM8*	145	DQ41	146	DQ45
13	DQ2	14	DQ6	79	CB2*	80	CB6*	147	DQS5	148	DM5
15	VSS	16	VSS	81	VDD	82	VDD	149	VSS	150	VSS
17	DQ3	18	DQ7	83	CB3*	84	CB7*	151	DQ42	152	DQ46
19	DQ8	20	DQ12	85	DU	86	DU	153	DQ43	154	DQ47
21	VDD	22	VDD	87	VSS	88	VSS	155	VDD	156	VDD
23	DQ9	24	DQ13	89	CK2*	90	VSS	157	VDD	158	/CK1
25	DQS1	26	DM1	91	/CK2*	92	VDD	159	VSS	160	CK1
27	VSS	28	VSS	93	VDD	94	VDD	161	VSS	162	VSS
29	DQ10	30	DQ14	95	CKE1	96	CKE0	163	DQ48	164	DQ52
31	DQ11	32	DQ15	97	DU	98	DU	165	DQ49	166	DQ53
33	VDD	34	VDD	99	A12	100	A11	167	VDD	168	VDD
35	CK0	36	VDD	101	A9	102	A8	169	DQS6	170	DM6
37	/CK0	38	VSS	103	VSS	104	VSS	171	DQ50	172	DQ54
39	VSS	40	VSS	105	A7	106	A6	173	VSS	174	VSS
				107	A5	108	A4	175	DQ51	176	DQ55
41	DQ16	42	DQ20	109	A4	110	A2	177	DQ56	178	DQ60
43	DQ17	44	DQ21	111	A1	112	A0	179	VDD	180	VDD
45	VDD	46	VDD	113	VDD	114	VDD	181	DQ57	182	DQ61
47	DQS2	48	DM2	115	A10/AP	116	BA1	183	DQS7	184	DM7
49	DQ18	50	DQ22	117	BA0	118	/RAS	185	VSS	186	VSS
51	VSS	52	VSS	119	WE	120	CAS	187	DQ58	188	DQ62
53	DQ19	54	DQ23	121	/CS0	122	/CS1	189	DQ59	190	DQ63
55	DQ24	56	DQ28	123	DU	124	DU	191	VDD	192	VDD
57	VDD	58	VDD	125	VSS	126	VSS	193	SDA	194	SA0
59	DQ25	60	DQ29	127	DQ32	128	DQ36	195	SCL	196	SA1
61	DQS3	62	DM3	129	DQ33	130	DQ37	197	VDDSPD	198	SA2
63	VSS	64	VSS	131	VDD	132	VDD	199	VDDID	200	DU
65	DQ26	66	DQ30	133	DQS4	134	DM4				

MODULE PIN DESCRIPTION

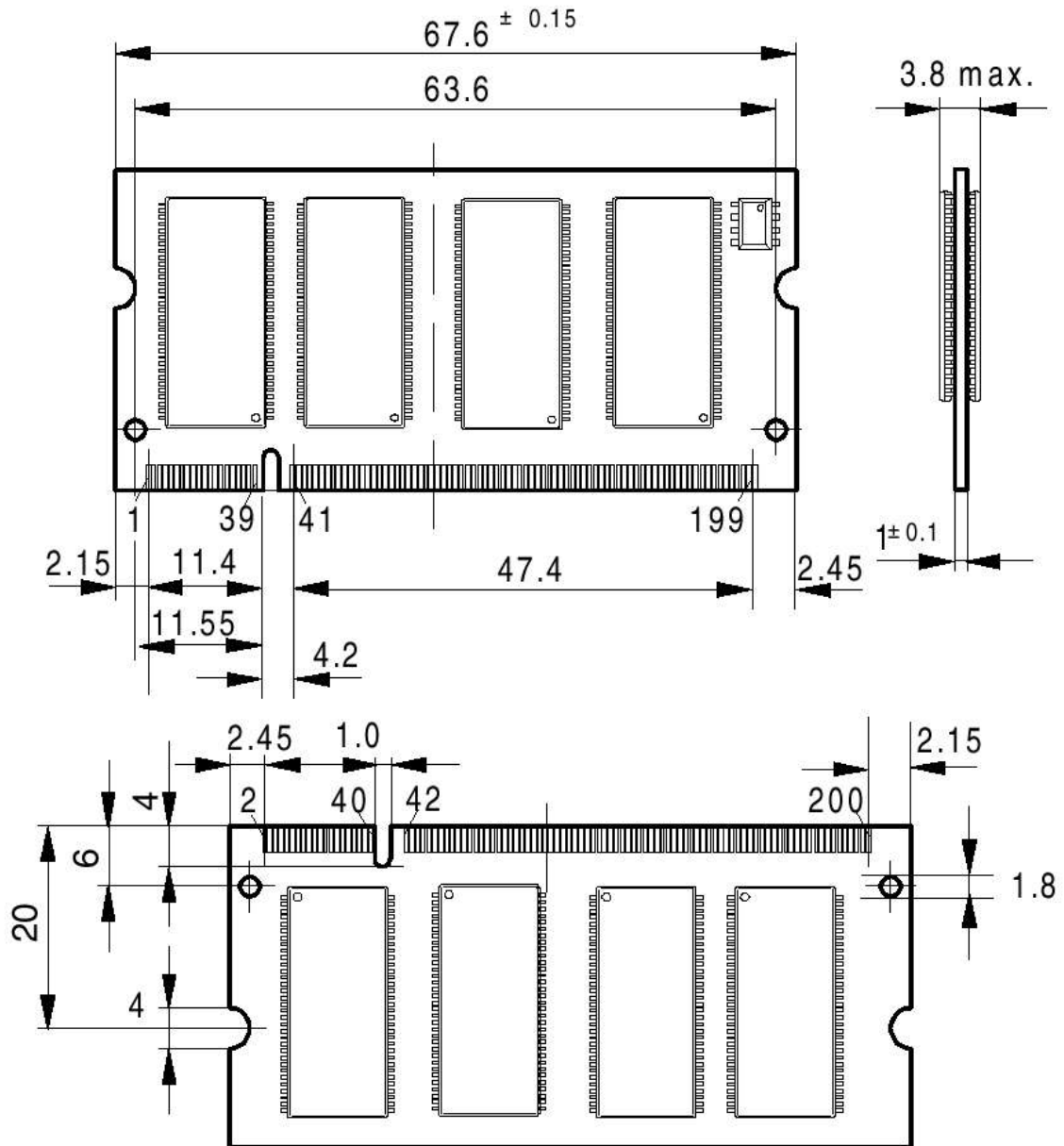
Pin	Description	Pin	Description
CK0,/CK0,CK1,/CK1,CK2,/CK2	Differential Clock Inputs	VDDQ	DQs Power Supply
CS0	Chip Select Input	VSS	Ground
CKE0	Clock Enable Input	VREF	Reference Power Supply
/RAS, /CAS, /WE	Command Sets Inputs	VDDSPD	Power Supply for SPD
A0 ~ A12	Address	SA0~SA2	E 2 PROM Address Inputs
BA0, BA1	Bank Address	SCL	E 2 PROM Clock
DQ0~DQ63	Data Inputs/Outputs	SDA	E 2 PROM Data I/O
DQS0~DQS7	Data Strobe Inputs/Outputs	VDDID	VDD Identification Flag
DM0~DM7	Data-in Mask	DU	Do not Use
VDD	Power Supply	NC	No Connection

LEGEND

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MODULE METROLOGY



Detail of Contacts

